

FIG. 1
(PRIOR ART)

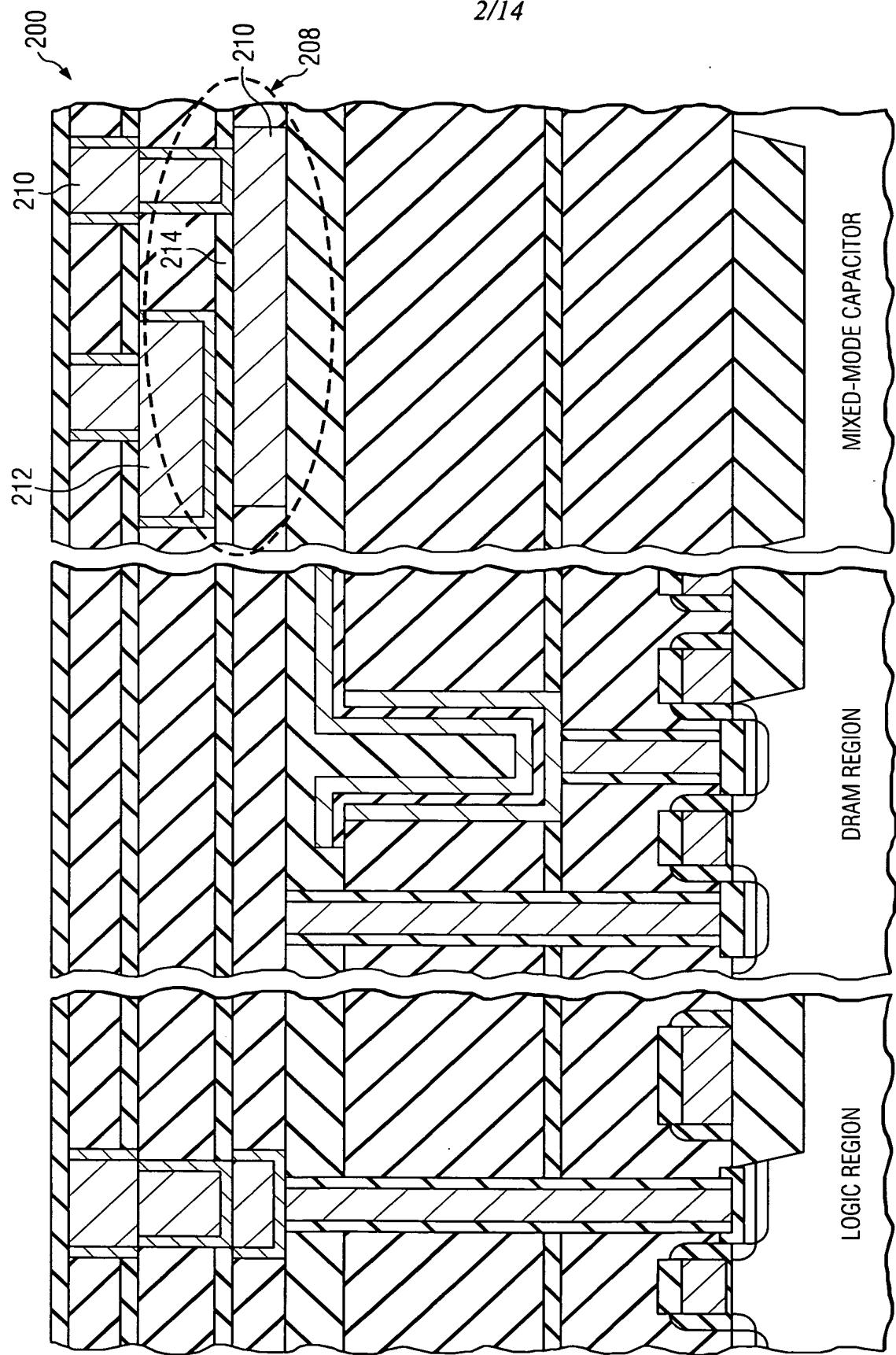


FIG. 2a
(PRIOR ART)

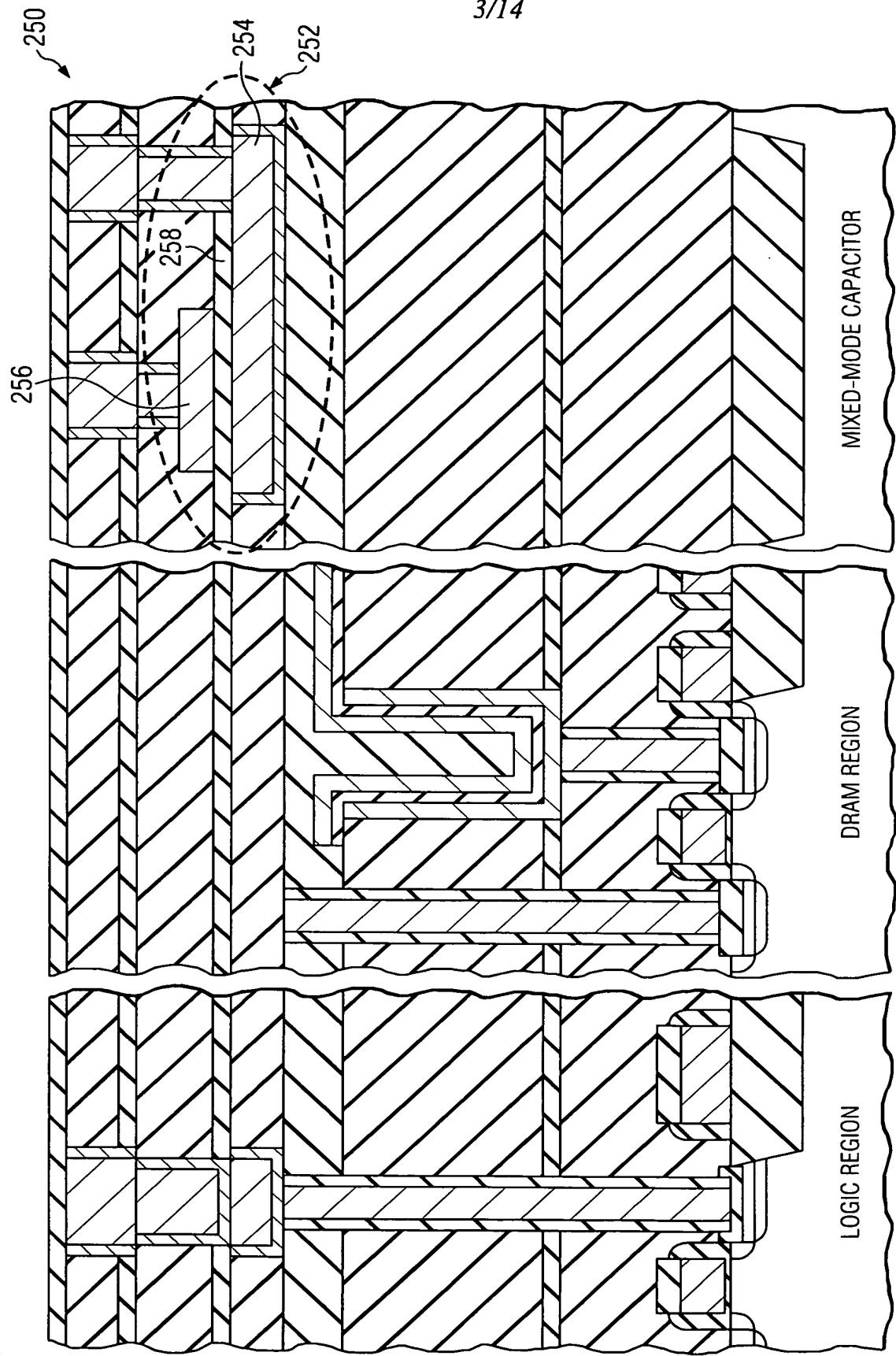


FIG. 2b
(PRIOR ART)

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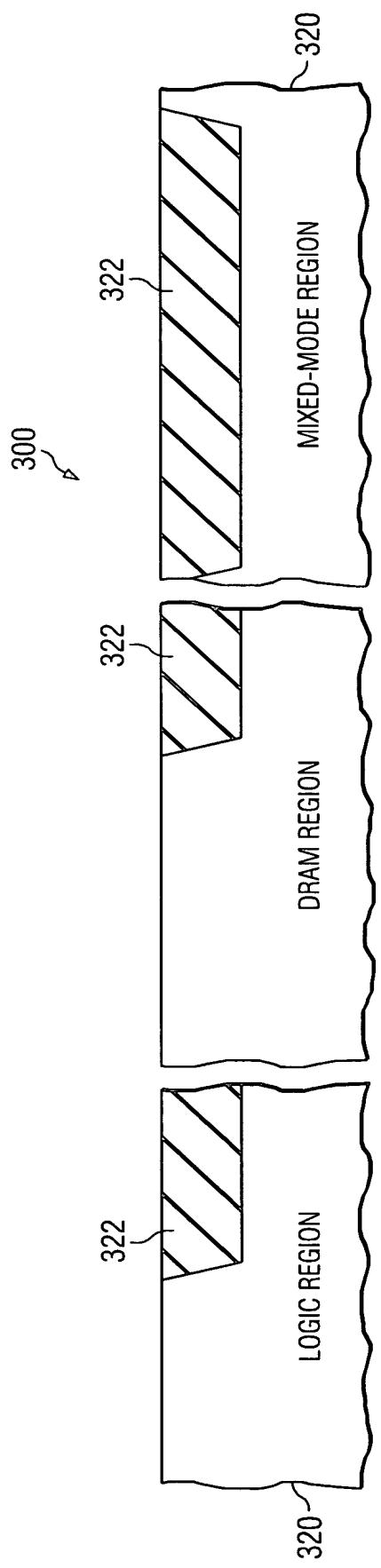


FIG. 3a

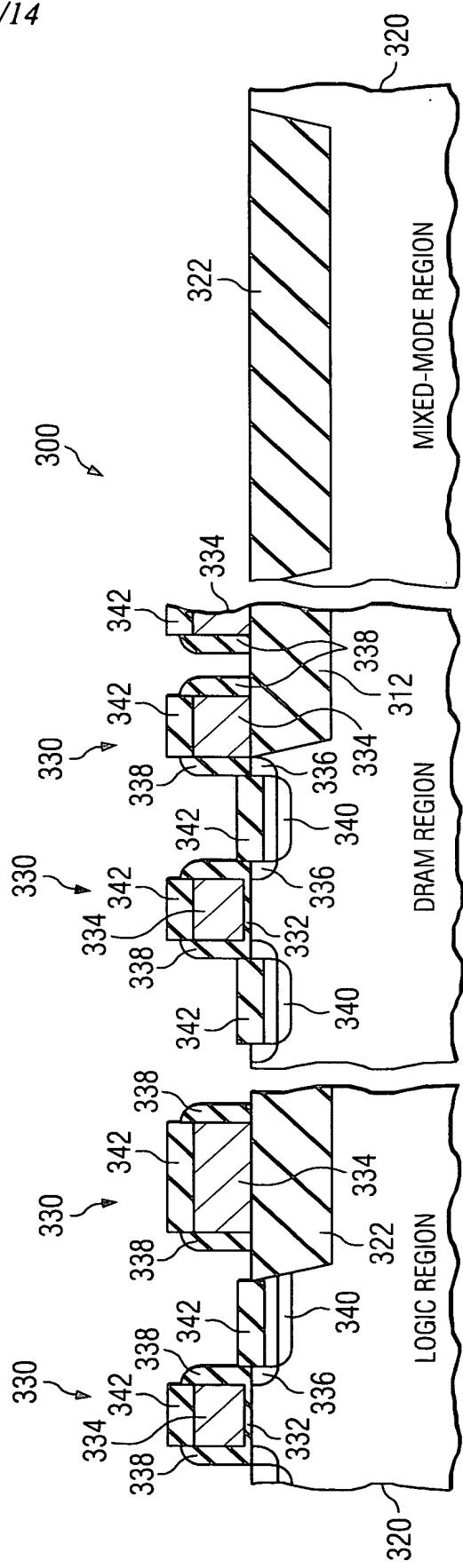


FIG. 3b

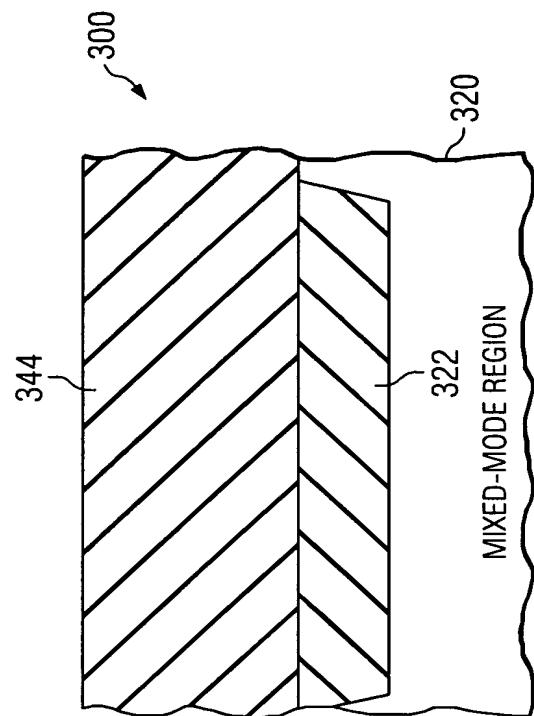
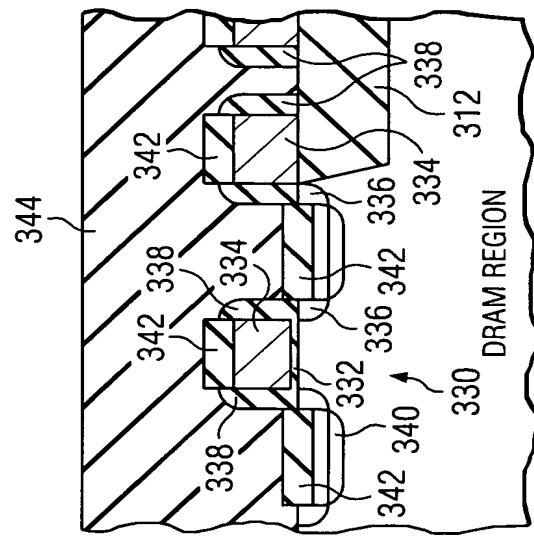


FIG. 3c



The diagram shows a rectangular area divided into several regions. Three specific regions are labeled with rectangles: one labeled 344 at the top left, one labeled 342 in the center, and one labeled 334 below it. The entire area is labeled "LOGIC REGION" on the right side.

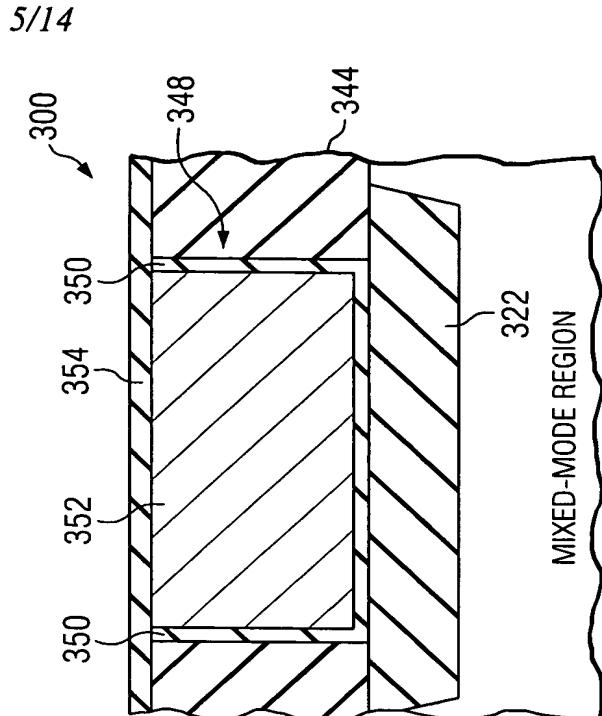
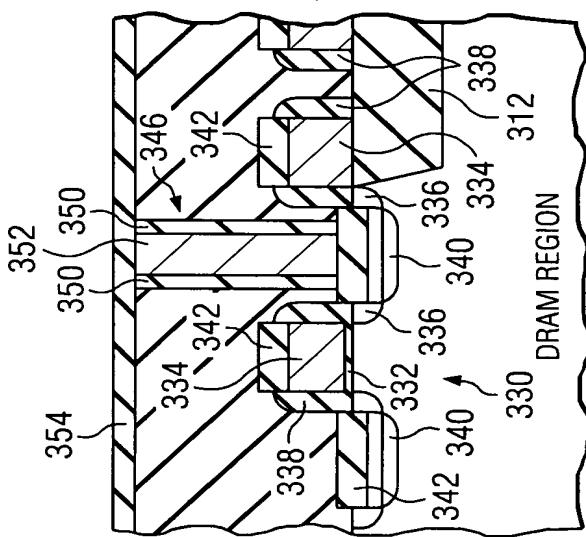


FIG. 3d



The diagram illustrates a logic region containing two memory blocks. The region is bounded by a wavy line labeled "LOGIC REGION". Inside, two rectangular blocks are shown with diagonal hatching. The top block is labeled "342" and the bottom block is labeled "334". To the left of the top block is the label "344", and below it is "354". To the right of the bottom block are labels "338", "334", "332", "336", "342", "340", "338", "334", and "322".

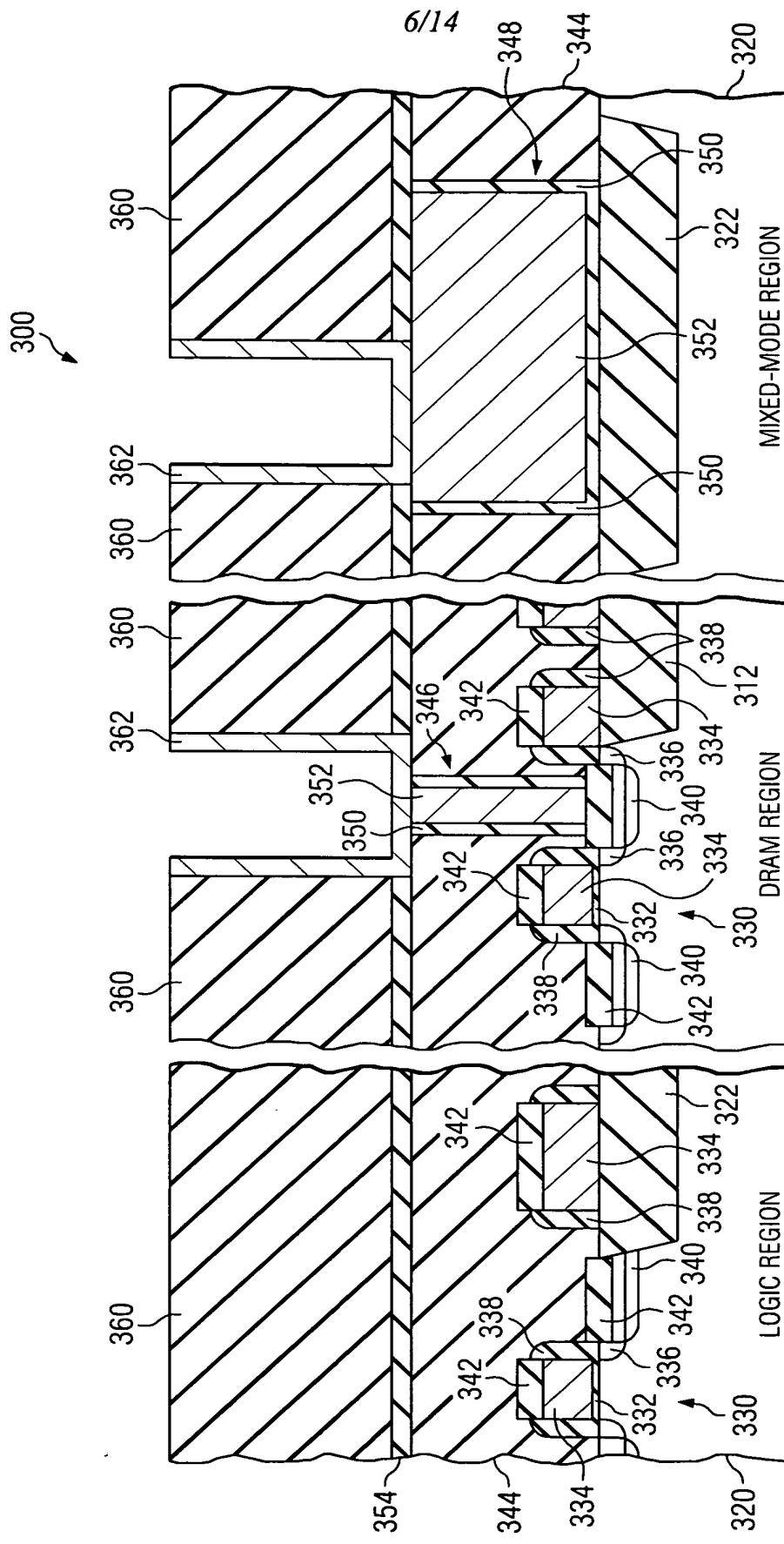


FIG. 3e

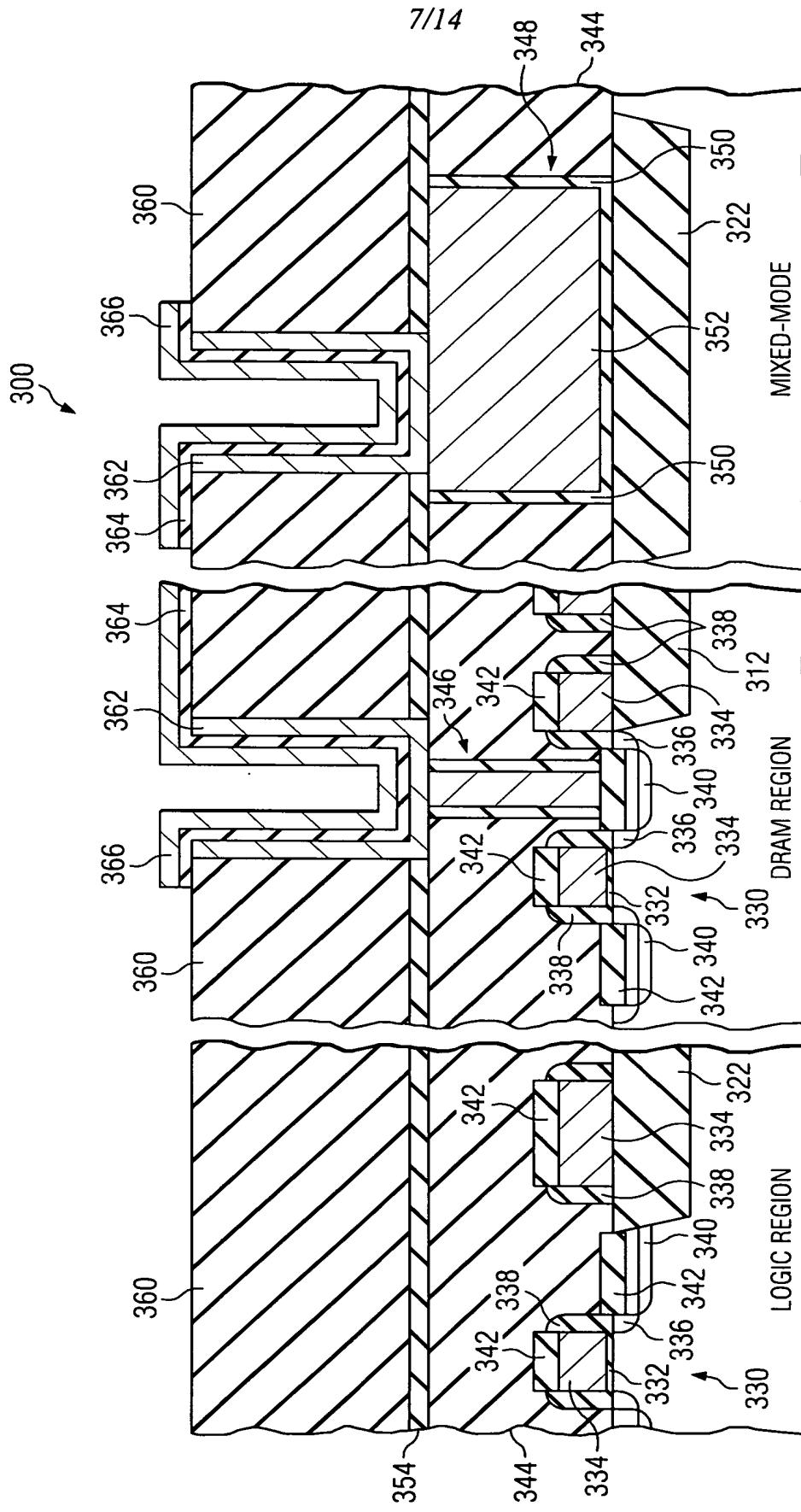


FIG. 3f

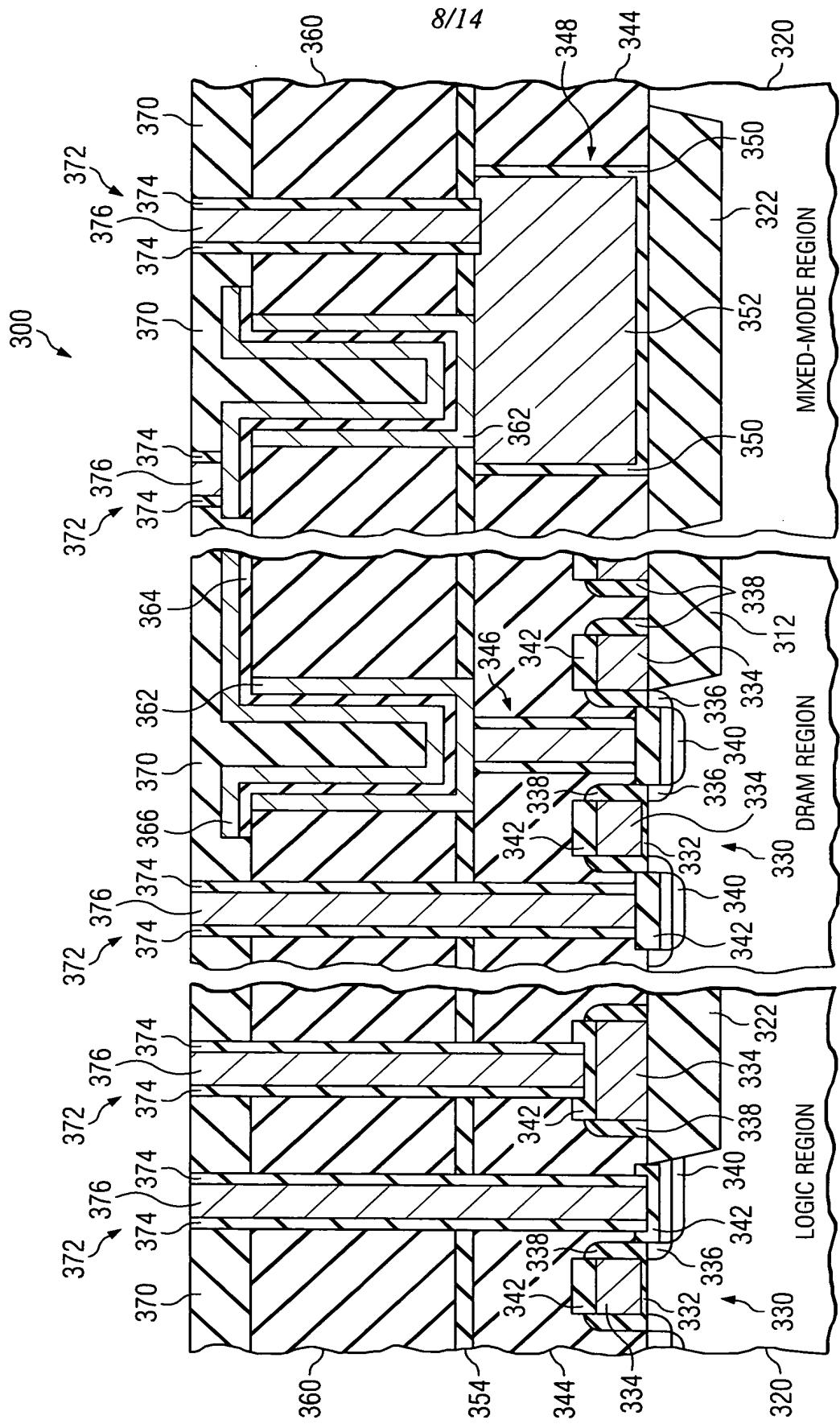


FIG. 3g

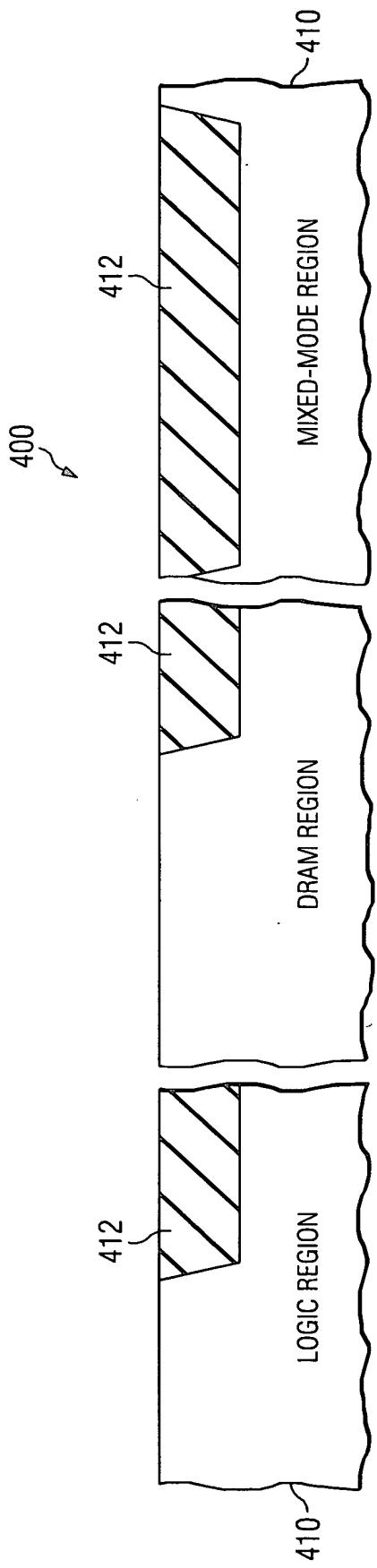


FIG. 4a

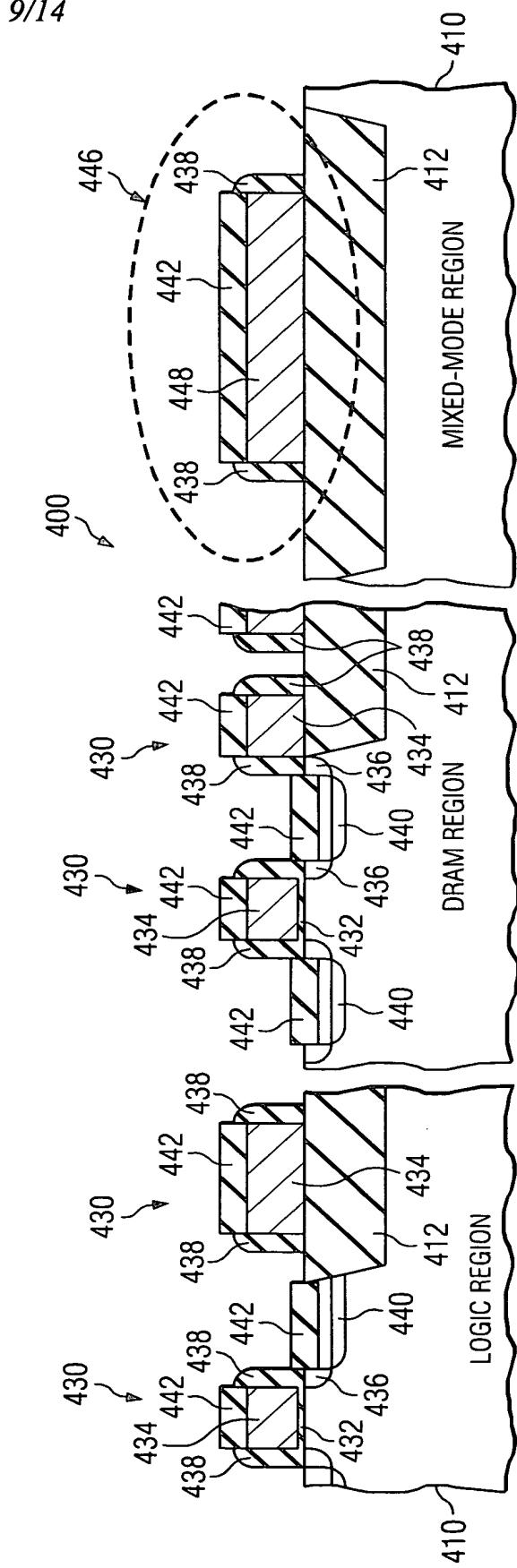


FIG. 4b

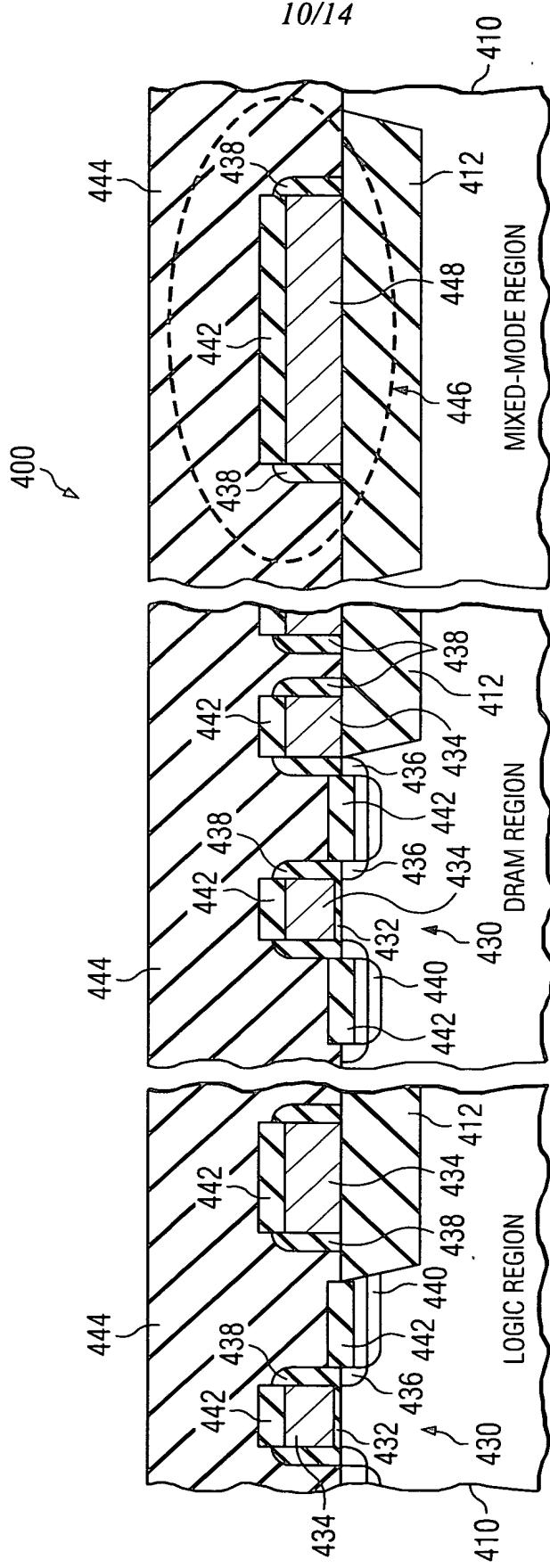


FIG. 4c

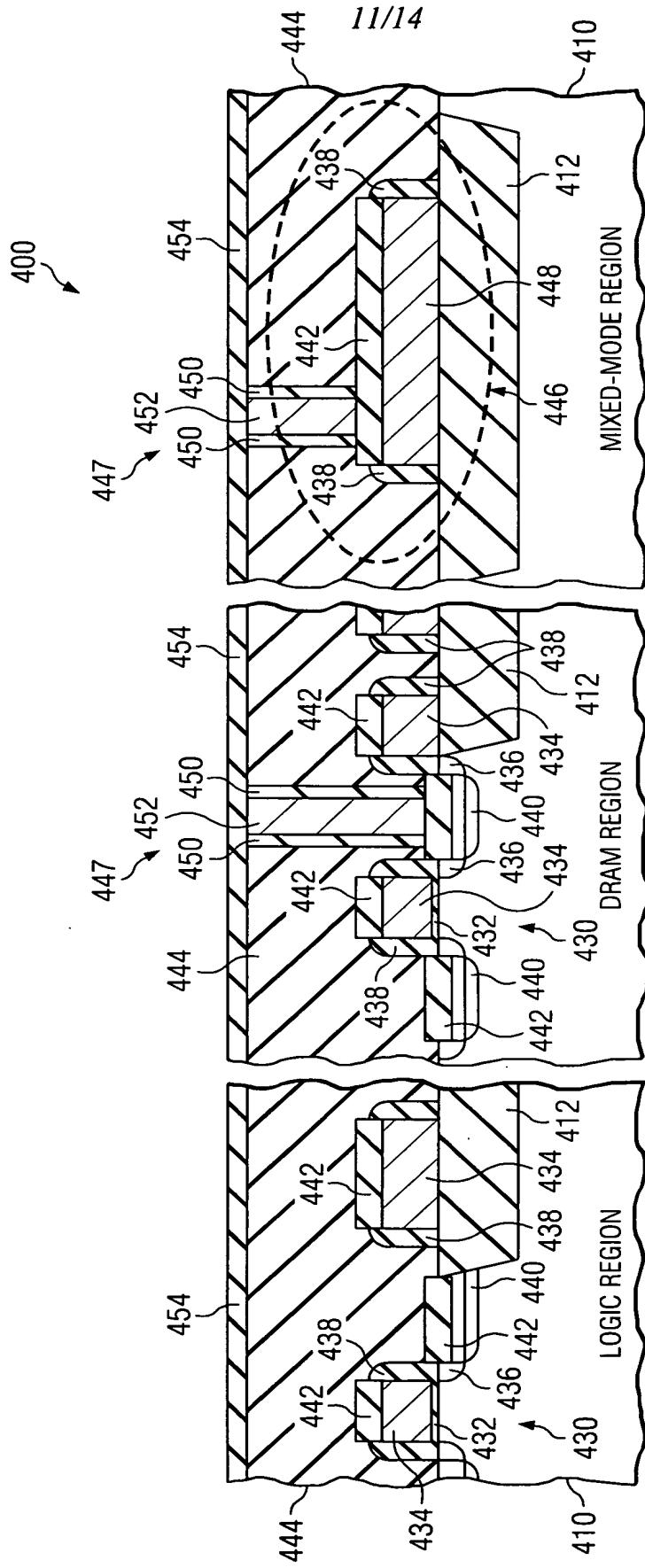


FIG. 4d

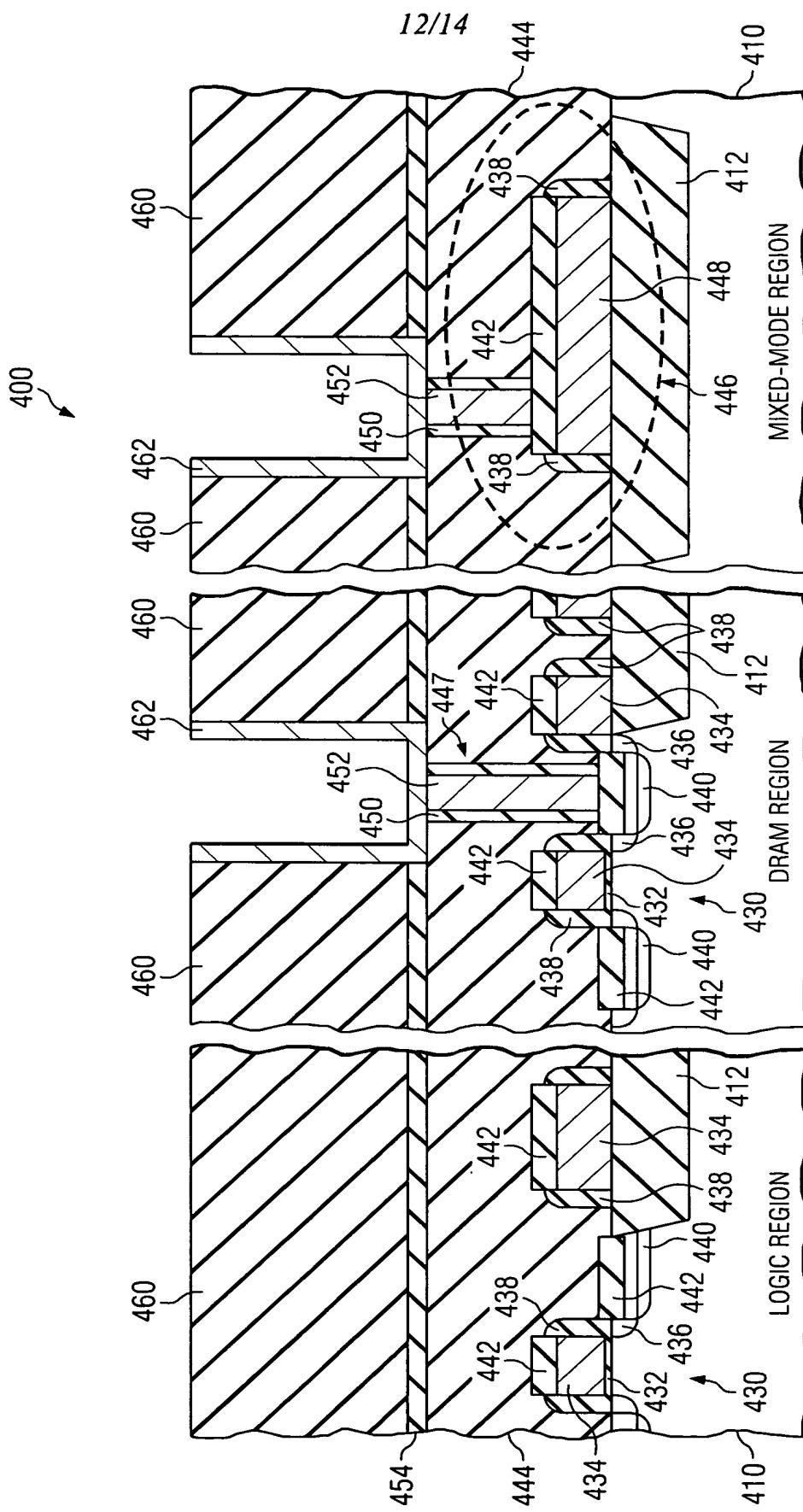


FIG. 4e

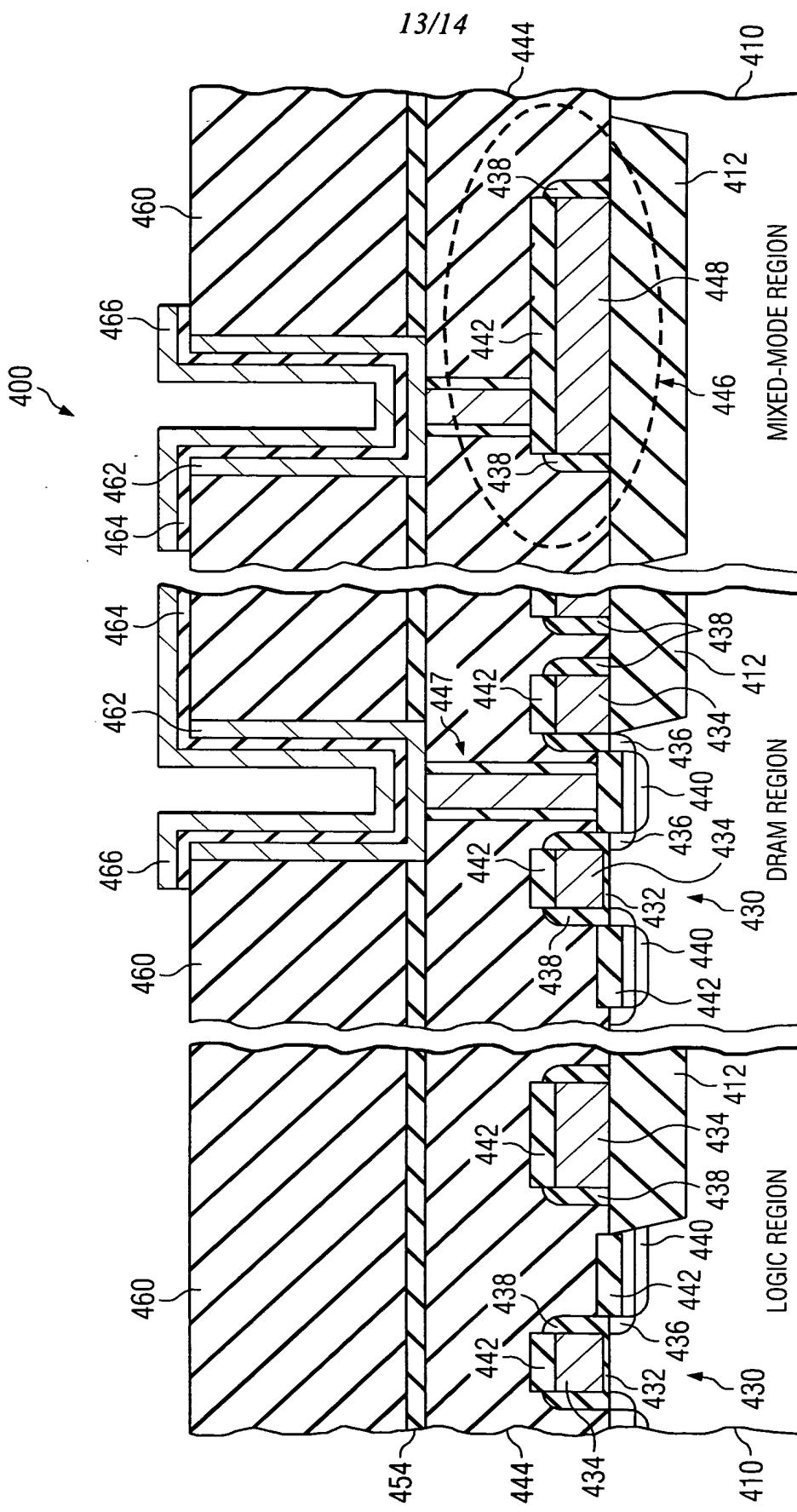


FIG. 4f

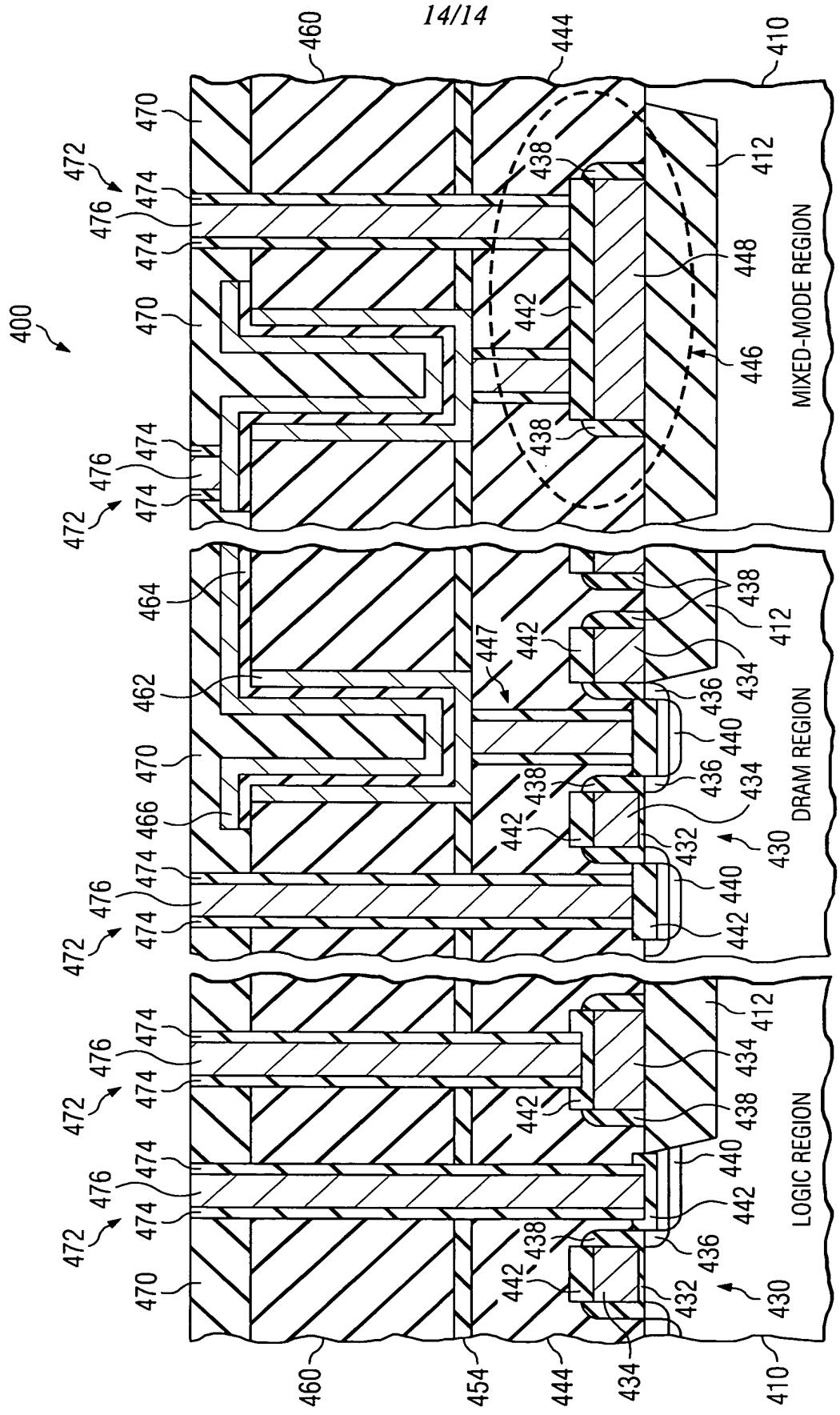


FIG. 4g